INSTRUCTION DESCRIPTION 1 (IE = "HIGH")

Table 6. Instruction Set 1

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear display	X	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return home	0	0	0	0	0	0	0	0	0	1	x	Set DDRAM address to "00H" from AC and return cursor to its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Power down mode	1	0	0	0	0	0	0	0	0	1	PD	Set power down mode bit. PD = "1": power down mode set, PD = "0": power down mode disable	39µs
Entry mode set	0	0	0	0	0	0	0	0	1	I/D	S	Assign cursor moving direction. I/D = "1": increment, I/D = "0": decrement and display shift enable bit. S = "1": make display shift of the enabled lines by the DS4 - DS1 bits in the shift enable instruction. S = "0": display shift disable	39µs
	1	0	0	0	0	0	0	0	1	1	B/D	Segment bi-direction function. BID = "0": Seg1 → Seg80, BID = "1": Seg80 → Seg1.	
Display ON/OFF control	0	0	0	0	0	0	0	1	D	C	B	Set display/cursor/blink on/off D = "1" : display on, D = "0" : display off, C = "1" : cursor on, C = "0" : cursor off, B = "1" : blink on, B = "0" : blink off.	39µs

Table 6. Instruction Set 1 (Continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Extended function set	1	0	0	0	0	0	0	1	FW	B/W	NW	Assign font width, black/white inverting of cursor, and 4-line display mode control bit. FW = "1": 6-dot font width, FW = "0": 5-dot font width, B/W = "1": black/white inverting of cursor enable, B/W = "0": black/white inverting of cursor disable NW = "1": 4-line display mode, NW = "0": 1-line or 2-line display mode.	39µs
Cursor or display shift	0	0	0	0	0	0	1	S/C	R/L	x	x	Cursor or display shift. S/C = "1" : display shift, S/C = "0" : cursor shift, R/L = "1" : shift to right, R/L = "0" : shift to left.	39µs
Shift enable	1	0	0	0	0	0	1	DS4	DS3	DS2	DS1	(when DH = "1") Determine the line for display shift DS1 = "1/0": 1st line display shift enable/disable DS2 = "1/0": 2nd line display shift enable/disable DS3 = "1/0": 3rd line display shift enable/disable DS4 = "1/0": 4th line display shift enable/disable.	39µs
Scroll enable	1	0	0	0	0	0	1	HS4	HS3	HS2	HS1	(when DH = "0") Determine the line for horizontal smooth scroll. HS1 = "1/0": 1st line dot scroll enable/disable HS2 = "1/0": 2nd line dot scroll enable/disable HS3 = "1/0": 3rd line dot scroll enable/disable HS4 = "1/0": 4th line dot scroll enable/disable.	39µs

Table 6. Instruction Set 1 (Continued)

Instruction	RE	Instruction Code										Description	Execution Time (fosc = 270kHz)
		RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Function set	0	0	0	0	0	1	DL	N	RE (0)	DH	REV	Set interface data length (DL = "1": 8-bit, DL = "0": 4-bit), numbers of display line when NW = "0", (N = "1": 2-line, N = "0" : 1-line), extension register, RE("0"), shift/scroll enable DH = "1": display shift enable DH = "0": dot scroll enable. reverse bit REV = "1": reverse display, REV = "0": normal display.	39µs
	1	0	0	0	0	1	DL	N	RE (1)	BE	0	Set DL, N, RE("1") and CGRAM/SEGRAM blink enable (BE) BE = "1/0": CGRAM/SEGRAM blink enable/disable	39µs
Set CGRAM address	0	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39µs
Set SEGRAM address	1	0	0	0	1	X	X	AC3	AC2	AC1	AC0	Set SEGRAM address in address counter.	39µs
Set DDRAM address	0	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39µs
Set scroll quantity	1	0	0	1	X	QC5	QC4	QC3	QC2	QC1	QC0	Set the quantity of horizontal dot scroll.	39µs
Read busy flag and address	X	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Can be known whether during internal operation or not by reading BF. The contents of address counter can also be read. BF = "1": busy state, BF = "0": ready state.	0µs
Write data	X	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM / CGRAM / SEGRAM).	43µs
Read data	X	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM / CGRAM / SEGRAM).	43µs

"X": Don't care